

**GENERAL**

Maximum Analog Test Points: 3200 or Maximum Digital Test Points: 1600  
 Operating System: Microsoft® Windows 2000/XP/Window 7 32Bit  
 Power Requirement: 200-240V, Single Phase, 50/60Hz 3KVA  
 Conforms to SMEMA standards  
 Air Requirement: Dry Air 4-8kg/cm<sup>2</sup>, Air Consumption: 4 liters/cycle  
 Fixture Type: Inline  
 Testable PCB Size: Standard: (W) 360 mm x (D) 300 mm x (H) 0.6-5 mm  
 Min. PCB Size: (W) 70 mm x (D) 70 mm  
 Component Height Limitations:  
 Top Surface of Conveyor: 90mm; Bottom Surface of Conveyor: 30mm

**ANALOG HARDWARE****Measurement Switching Matrix: 6-wire measurement**

Programmable Frequency: 100Hz, 1KHz, 10KHz, 100KHz, 1MHz  
 Programmable DC Voltage Source: ±10V max, Resolution: 6.1mV  
 Programmable DC Current Source: +100mA max, Resolution: 0.2mA  
 Programmable AC Voltage Source: 10Vpp max, Resolution: 6.1mV  
 Programmable High Voltage DC Source: 43V@43mA max

**Component Measurement Capability**

Resistance: 1ohm-40Mohm  
 Capacitance: 10pF-40mF  
 Inductance: 10µH-60H

**Analog Measurement**

AC Voltmeter: 0-100V  
 DC Voltmeter: 0-±100V; Resolution: 2.5mV-50mV  
 DC Ampmeter: 1µA-160mA; Resolution: 30nA-30µA

**OPTIONAL HARDWARE****Analog Test**

TestJet Technology: Vectorless open circuit detection  
 Arbitrary Waveform Generator (AWG): Frequency Range 0-100KHz; Resolution: 0.15Hz

**Digital Test**

Non-multiplexing 1:1 per pin architecture  
 Pin Drivers: Programmable levels 0.5V to 4V  
 Pin Receivers: Programmable levels -5V to 5V  
 Pull-up/Pull-down Resistor: 4.7K  
 DUT Power Supplies: 5V@3A, 3.3V@3A, 12V@3A, 18V@3A, -12V@1A and 24V@3A  
 Programmable DUT Power Supplies: 25V@ 8A, 75V@ 2.5A  
 On-board Programming of Flash & EEPROM Memories  
 MAC Address Programming: Supports MAC address programming with server supplied MAC address  
 Boundary Scan: Includes B-Scan Chain Test, B-Scan Cluster Test, B-Scan Virtual Nails Test and IEEE1149.6 Test  
 ToggleScan Test: Advanced test technology that combines with B-Scan and Vectorless test functions to detect pin open or short issues  
 Tree Test Facilities with BGA Test: Pattern generator for detection of pin opens for BGA/VLSI chips

**DIMENSIONS & WEIGHT**

Dimensions: (W) 900 mm x (D) 900 mm x (H) 1640-1840 mm  
 (not including signal tower, signal tower height: 515 mm)

Weight: 500kg  
 Conveyor Height: 890-1100 mm

**POWERFUL SOFTWARE ENVIRONMENT**

Microsoft® Windows operating system software; User-friendly interface  
 Automatic Test Program Generator (ATPG)  
 Automatic protection of specific points during debug  
 Auto-learning and test program generation for opens/shorts clamping diode and TestJet tests  
 Auto-debugging of passive components  
 Built-in self-diagnostic function  
 Board view displays test fail devices and pins instantly

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T R 5 0 0 1 I N L I N E I C T



- AUTOMATED INLINE IN-CIRCUIT TEST SYSTEM
- FULLY UPGRADABLE FROM MDA TO ICT
- COST-EFFECTIVE DIGITAL 1:1 DRIVER/RECEIVER PER PIN ARCHITECTURE DESIGN
- POWERFUL BOUNDARY SCAN TEST SOLUTIONS
- EASY TO USE ON BOARD PROGRAMMING SOFTWARE

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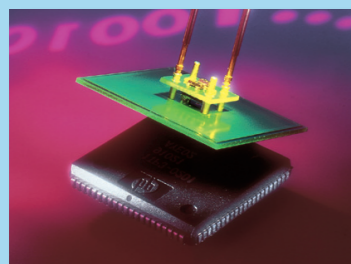
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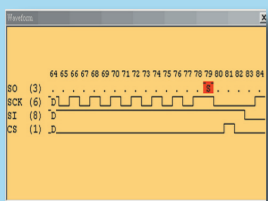
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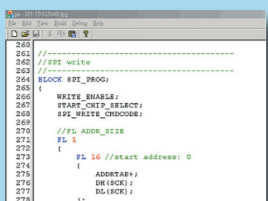
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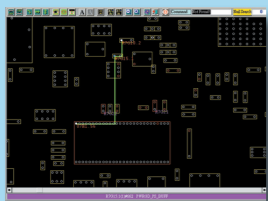
TestJet Technology



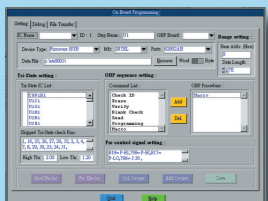
Waveform display



Color syntax program editor



Board view with trace display capacity



Flash programming

ANALOG TEST

HIGH PERFORMANCE MANUFACTURING DEFECTS ANALYZER (MDA)

RLC MEASUREMENT

- 6-Wire Measurement
- Auto-Guarding Feature
- AC Phase Measurement
- High-Speed Test

TESTJET TECHNOLOGY

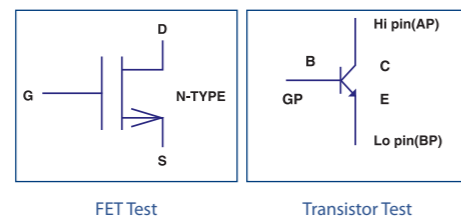
Detects open connections on ICs, connectors and other SMT devices.

CAPACITOR POLARITY TEST

- Leakage Current Measurement
- TestJet Detection

TRANSISTOR / DIODE MEASUREMENT

- Diode
- Zener Diode
- Transistor: PNP, NPN
- FET/SCR/TRIAC
- Photo Coupler



DIGITAL TEST

FULL DIGITAL IN-CIRCUIT TEST (ICT)

USER FRIENDLY INTERFACE

The TR5001 provides an easy to understand and flexible interface.

- Color syntax program editor
- C-like test language
- Editable waveform display tool
- Integrated development environment

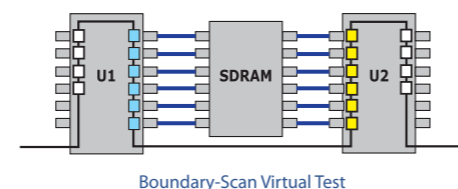
EASY-TO-USE ON-BOARD PROGRAMMING SOFTWARE

Modularized memory algorithms on board programming.

- Flash Programming
- Serial Device Programming

POWERFUL BOUNDARY-SCAN CHAIN TEST CAPABILITY

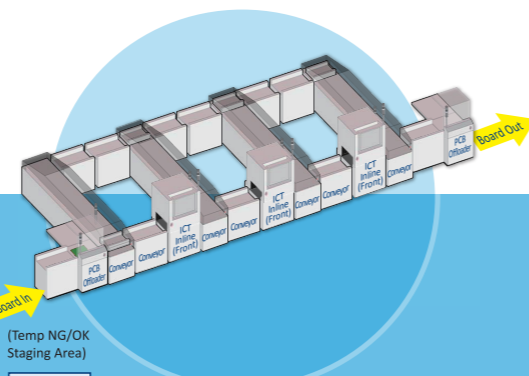
Auto-generation of test programs and reports through the boundary scan Test Program Generator (BSTG) incorporate different types of test categories like individual boundary scan device tests, boundary scan device chain tests, virtual nail tests for RAM, ROM, TTL & TREE devices, and IEEE1149.6 tests.



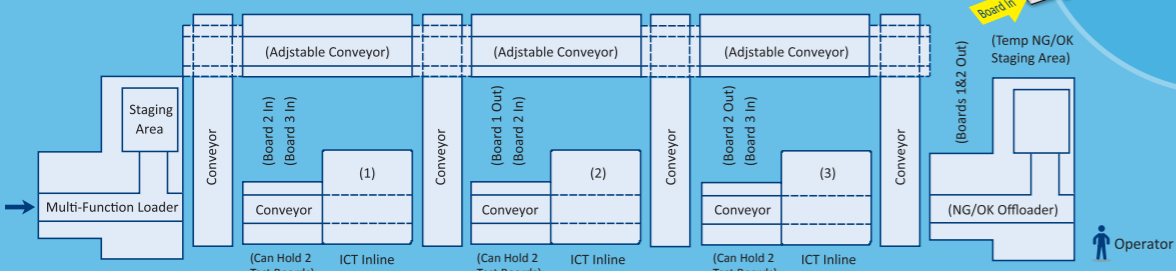
THE MOST COST-EFFECTIVE TEST STRATEGY

Non-Multiplexing Pin Design; Driver/Receiver to Pin Ratio 1:1

- Optimized nail placement with 1:1 ratio flexibility
- ECNs only require moving few existing wires compared with 2:8/2:9 driver/receiver per pin
- 1:1 Driver/Receiver per pin provide the fastest test program development and debugging

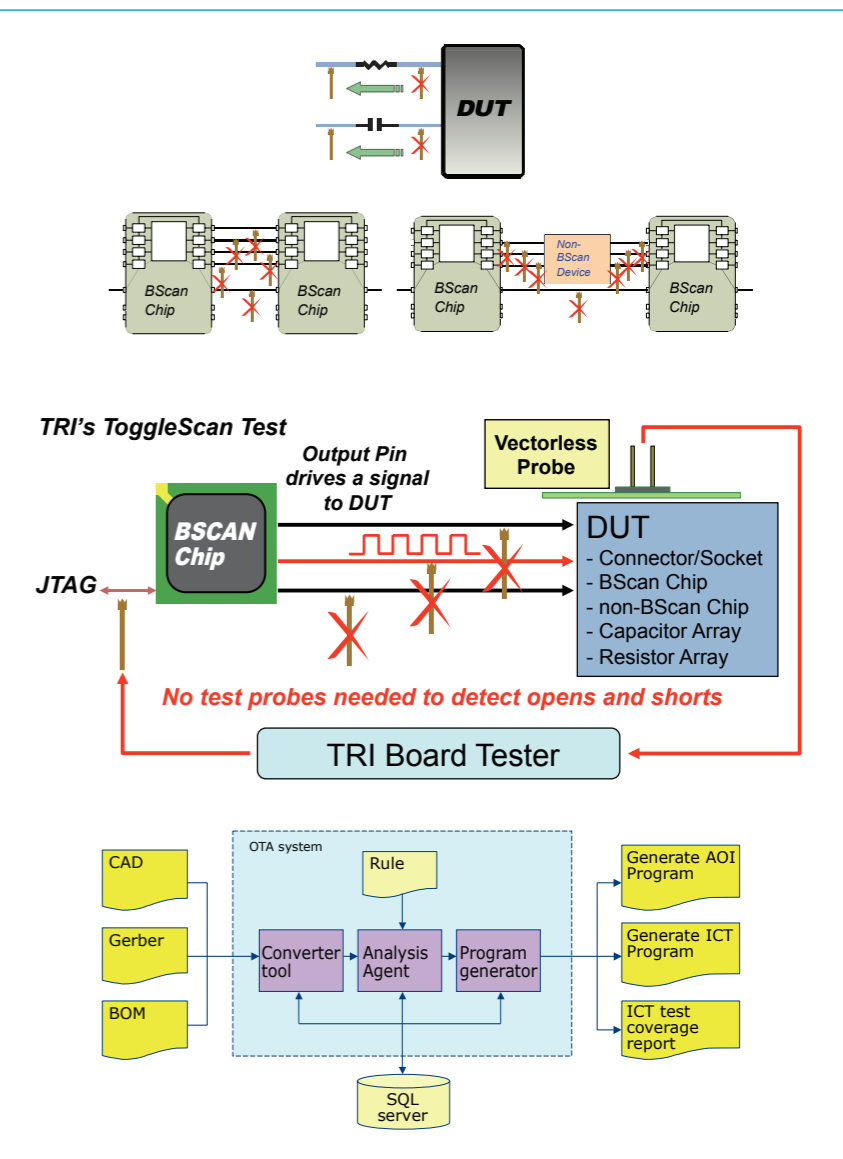


PRODUCTION LAYOUT MOTION



NO ACCESS SOLUTION

- Drive Through Test
- Boundary Scan Test
- TRI ToggleScan Test  
TRI's patented ToggleScan technology is the perfect solution for current and future generations of component-dense PCBAs with little or no test access. Fully compliant with the draft IEEE 1149.8.1 standard, ToggleScan provides maximum test coverage by detecting opens and shorts on many kinds of devices, including connectors, sockets, boundary scan and non-BScan chipsets, differential AC-coupled signal chipsets, resistor arrays and capacitor arrays.
- TRI CPU Socket Test
- Optimal Test Analyzer (OTA)

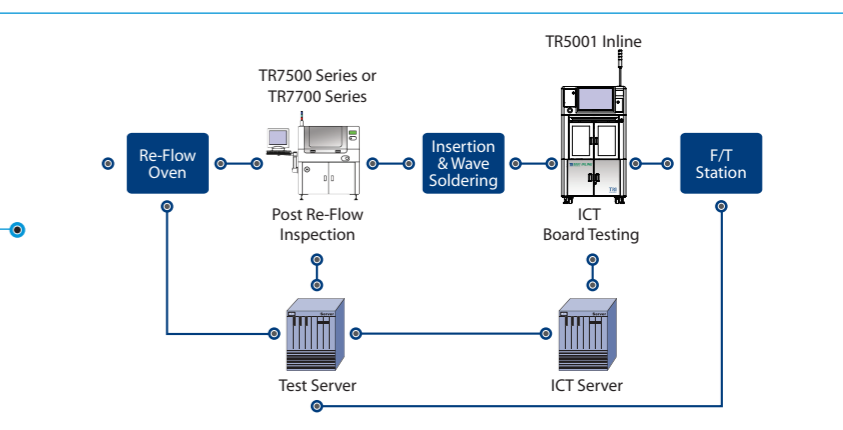


SHOP FLOOR SYSTEM SUPPORT

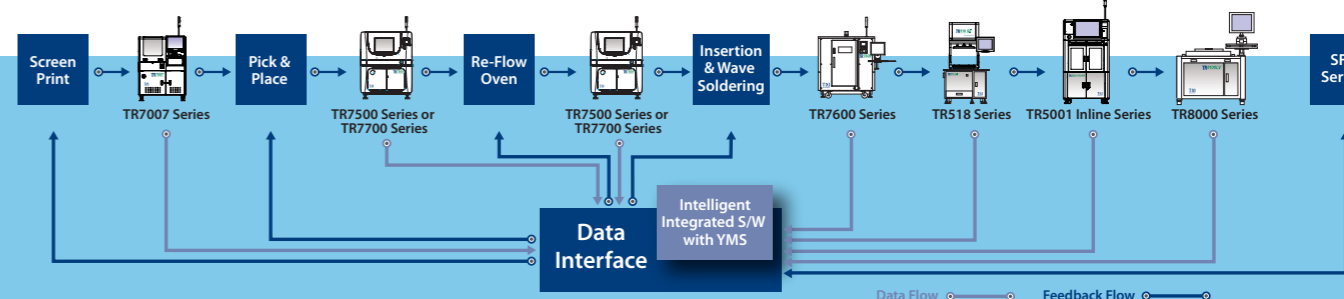
- Supports text file, data base, and DII interfaces
- S/N and operator ID check
- Multi-data exchange protocol

INLINE FIXTURE DESIGN

- Fast-insertion mechanism
- Conforms to SMEMA standards
- Dual stage press unit
- Fast, easy fixture swap
- Reduced labor costs
- Increased productivity
- Enhanced efficiency
- Automatic test without human interruption
- Test program compatibility with TR5001/TR5001E
- Semi-automatic fixture Installation
- PCBA protection mechanics



YIELD MANAGEMENT SYSTEM \*



- Testers enable process capability control
- Real-time defect information integration and analysis
- Defect knowledge management

\*Optional